Advanced electronic equalization and signal processing for optical communication

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Outline

- Introduction
- Signal impairments in optical communication systems
- Electronic equalization schemes
  - FFE and DFE
  - Viterbi equalizer
- Advanced electronic equalization concepts
- Conclusions
Introduction

- State of the art optical transmission systems are operated close to optimum
- Typical system margins are in the range of few dB in OSNR (1 dB … 3 dB) allowing a very low degradation, only
- Degradation of system performance is due to limited perfection of transmitter, fiber link and receiver including ageing
- Drivers for future
  - Increase of data volume
  - Decrease of cost
  - Availability of appropriate microelectronics technology
1 Signal impairments in optical communication systems
Signal impairments in optical communication systems

Optical transmission systems suffer from
Limitation of system performance by signal impairments

- transmitter
- transmission channel
- receiver

Task of electronic dispersion compensation (EDC)
- mitigation of all impairments to improve system performance
Signal impairments in optical communication systems

Impairments from transmitter
- Limited bandwidth
- Extinction ratio (9 ... 12 dBm)
- Chirp
Signal impairments in optical communication systems

Impairments from transmission channel

- Noise accumulation
- Limitation bandwidth of optical channel 40 Gb/s w. 50 GHz spacing
- Chromatic dispersion 10 Gb/s - uncompensated links
  40 Gb/s - decreased CD tolerance
- PMD especially in older fibers
- SPM if launch power > 0 dBm
- XPM
- FWM
Signal impairments in optical communication systems

Impairments from receiver
- Limited bandwidth
- Noise (w. and w/o. optical amplifiers)
2 Electronic equalization schemes
Electronic equalization schemes

Transmitter and receiver equalization schemes

**transmitter**

**receiver**
Electronic equalization schemes

Transmitter and receiver equalization schemes

- Adaptation

For many applications EDC in receiver is optimum
Electronic equalization schemes

Transmitter based EDC - Electronic predistortion

- Generation of precompensated optical field
- Independent modulation of I and Q

- Chipset solution, but very complex Tx
- Adaptation: feedback via reverse channel
- More than 5000 km w/o. DCM
- Sensitivity to non-linearity’s
  - A. Klekamp, “Nonlinear Limitations of Electronic Dispersion Pre-Compensation by Intrachannel Effects“ OFC’06, OWR1, see also OWB1 OFC’06
Electronic equalization schemes

Receiver based EDC

- Analog and digital approaches after o/e conversion

- Application of FFE and DFE
  - Several prototypes for 10 Gb/s
  - First circuits reported at 40 Gb/s
    - StrataLight, Alcatel

- ADC
  - Equalization of signal in DSP (Viterbi algorithm)
  - First prototypes reported at 10 Gb/s
    - CoreOptics, Intersymbol Comm.
Electronic equalization schemes

Comparison of analog and digital equalizers

- Sensitivity to GVD and PMD for NRZ at 10 Gb/s

- Standard receiver with 5 GHz bandwidth
- VE 10 GS/s with BW of 3.5...5 GHz, 20 GS/s w. 6...8 GHz
- Similar behaviour for equalizers for low distortions or low penalty range
- VE outperforms FFE/DFE at higher distortions
FFE and DFE

Realization of analog equalizers

**FFE**

- 40 Gb/s FFE with 5 taps
  - SiGe technology
  - area 2.0 x 1.5 mm², <2W power diss.

**DFE**

- 1 bipolar tap weight, 1 bit period delay

FFE and DFE are feasible up to 40 Gb/s, technology CMOS and SiGe
FFE and DFE

Adaptation of analog equalizers

- LMS algorithm for FFE/DFE

- LMS algorithm not optimum for optical noise loaded signals
- LMN improves performance, difficult for implementation
- Highest speed adaptation for FFE and DFE up to MHz range
FFE and DFE

Eye monitor feedback for analog equalizers

- Eye monitor available for 10 and 40 Gb/s application
- Requires sequential adaptation of tap weights
  - Improved performance of EDC at reduced adaptation speed

PER = $10^{-3} \ldots 10^{-1}$
FFE and DFE

Performance of analog equalizer realization (FFE)
- 42.7 Gb/s NRZ
- Simulations with optimum adaptation
- Experiments with manually optimized parameters

- Performance close to theoretical limits
- Suitable for transponder integration
Viterbi equalizer

Digital equalization: Viterbi equalizer at 10 Gb/s

- ADC with 3 to 4 bit resolution
- Sampling with 10 to 20 GS/s
- Viterbi equalization with 4 states
- Determination of most probable sequence
Viterbi equalizer

ADC with flash architecture
- 10 GS/s ADCs are feasible
- beyond 10 GS/s
  - 3 bit at 20 GS/s in SiGe, CoreOptics
  - 8 bit 20 GS/s in 0.18µm CMOS
    Agilent, power dissipation 10 W
  - 3 bit 40 GS/s in 0.12µm SiGe
    TelASIC, power dissipation 3.8 W
- not reported: >>10 GHz bandwidth
- 40 Gb/s requirements
  - DQPSK: 20 GS/s, 15 GHz bandwidth
  - NRZ and PSBT: 40 GS/s, 30 GHz bandwidth
Viterbi equalizer

Architecture of Viterbi core

- ACS is most time critical building block in realization

Branch metric $\gamma_{0,k}$
State metric $\lambda_{00,k}$

Simulations: $512\text{ps} + 15\text{ps} + 512\text{ps} + 80\text{ps}$ (CMOS 130 nm)
Sum: $1,119\text{ns}$ -> max clock frequency of substrate: $890\text{ MHz}$

Parallelization of algorithm necessary
Viterbi equalizer

Parallel architecture of Viterbi equalizer

- Minimized Method (Sliding Window method very similar)

Input 10 Gb/s

1st best state estimation

2nd best state estimation

Trace back

n bits in parallel
2 x trace back length

3 x trace back length

Data Output Soft Output

Input Samples q bits wide

Processing 622 Mb/s

Output 10 Gb/s
Viterbi equalizer

Parallel architecture of Viterbi equalizer

- Minimized Method (Sliding window method very similar)

\[ 2 \times m \times \text{trace back length} \]
Viterbi equalizer

Parallel architecture of Viterbi equalizer
- complexity of full matrix

$x = \text{number of states}$
Viterbi equalizer

Parallel Viterbi equalizer realization at 10 and 40 Gb/s:
- Minimized method or Sliding window: estimation of building block count

<table>
<thead>
<tr>
<th>Boundary conditions</th>
<th>Hardware effort</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trace back length of algorithm</td>
<td>Subrate [MHz]</td>
</tr>
<tr>
<td>10 Gb/s</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>8</td>
</tr>
<tr>
<td>40 Gb/s</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>8</td>
</tr>
</tbody>
</table>

- High number of building blocks, but pure digital
- Consider: 256 ACS units - power dissipation < 2 W
Viterbi equalizer

Adaptation of Viterbi equalizer

“channel model” for VE adaptation

- Pdf’s can be extracted from conditional histograms
- Adaptation is realized as digital subfunction
- Max. speed up to 1MHz
Viterbi equalizer

Performance of digital equalizers

- 10.7 Gb/s, NRZ
- Automatic adaptation in experiment

- Performance close to theoretical limits
- Suitable for transponder integration

3 Advanced equalization schemes
Advanced EDC concepts

Viterbi equalization with oversampling

- Application of 2 S/bit - already realized by CoreOptics

Correlation sensitive algorithm

- Cope with noise correlation in bandwidth limited systems (OFC’05, OFO 2) see also OWB6 OFC’06
Advanced EDC concepts

Viterbi equalization for 2 input signals (e.g. DQPSK)

- M. Cavallari, OFC‘04, TuG2

- DQPSK requires 2 receivers
- joint symbol VE for both channels (I and Q)
EDC applications

EDC for DPSK and DQPSK modulation format at 40 Gb/s

- Lower improvement of performance by EDC for DPSK and DQPSK
EDC applications

EDC for advanced Viterbi equalization of DQPSK
- very attractive for 40 Gb/s
  - System simulations for DQPSK
    - M. Cavallari, OFC’04, TuG2

 feasable approach w. 2x20 GS/s
 @ 2dB penalty

 CD tolerance of 350 ps/nm seems to be possible at 40 Gb/s
EDC applications

EDC in PSBT systems (very attractive for 10 and 40 Gb/s systems)

- Viterbi: 1 S/bit - 40 GS/s feasibility has to be proven
  2 S/bit - not feasible
- Simulations w. standard PSBT @ 10.7 Gb/s (OFC 05, OThJ4)

- Limited improvement by EDC
- Tolerance: >200 ps/nm @ 40 Gb/s
Advanced EDC concepts

Improved architecture for FFE/DFE

- Application of non-linear taps
  C. Xia, “Performance enhancement for duobinary modulation through nonlinear electrical equalization”, ECOC 2005, Glasgow, 4.2.3.

- Non-linear FFE/DFE outperforms linear FFE/DFE and VE
- Requirements on circuit, adaptation?
Coherent DSP equalization

- conversion of phase / polarization information of distorted signal into the electrical domain
- numerical equalization (DSP) of CD, PMD, (SPM) after analog-to-digital conversion possible (ADC: 2 samples/symbol)

\[
I = E_{\text{signal}}^{\text{TE}} \times E_{\text{LO}} \\
Q = E_{\text{signal}}^{\text{TE}} \times (E_{\text{LO}} \times e^{i\pi/2})
\]

e.g.:
- S. Tsukamoto et al., OFC/NFOEC2006, OWB4: DQPSK, 20Gb/s
- S.J. Savory et al, ECOC 2006, Th2.5.5: 40G pol. multiplexed QPSK, 10Gbaud
- S. Tsukamoto, K. Kikuchi et al., ECOC 2006, Mo4.2.1
Mitigation of CD (>3000 km SMF) and PMD (up to 25 ps DGD) possible
Tx and Rx signal processing

OFDM with Tx and Rx signal processing

- **OFDM setup**

  - IFFT and DAC in Tx
  - ADC and FFT in Rx
  - Realization of all components seems to be feasible
Tx and Rx signal processing

Simulations

- A. Lowery, OFC 2006, Anaheim, PDP39
  32x10 Gb/s 4000 km without DCM, limit of transmission length by nonlinearities and noise
- W. Shieh, Electronics Letters, 42(11)2006
  Coherent optical OFDM: improvement of sensitivity, but same dispersion tolerances
  No penalties by CD up to 34.000 ps/nm dispersion

- I. Djordjevic, IEEE PTL 18(15)2006
  100 Gb/s @ 25 GHz optical bandwidth, comparison of QPSK and 16-QAM, QPSK outperforms 16QAM, up to 2900 km simulated

Demonstration

- 20 Gb/s transmission with offline processing by KDDI and Monash Univ. (OFC 2007, PDP)
Conclusions

- Performance of electronic processing schemes are close to theoretical limits even at 40 Gb/s
- Realization of analog and digital equalizers are feasible
- Required microelectronics technology is available
- Electronic signal processing increases dispersion tolerances and system robustness
- Suitable approach for channel based application in commercial transponders